Agilent E9522A
Freescale StarCore140
Nexus Decoder

Design Guide

Agilent Technologies

Notices

Manual Part Number

E9522-97000

This manual is available online at www.agilent.com. It is not an orderable part.

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1 Introduction

In This Guide...

This *Design Guide* provides information to assist you in designing a board which will be compatible with the Agilent E9522A Freescale StarCore140 Nexus Decoder. It tells you what signals are required by the decoder, and suggests how to route these signals to a header.

For information on using the decoder, see the online help which is installed with the decoder.

Product Overview

The Freescale StarCore140 Nexus Decoder, used with an Agilent Technologies logic analyzer, allows you to decode and view messages from an SC140 DSP core in your target system.

The decoder can decode 2-, 4-, 8-, 16-, 30-, and 32-bit wide data. (The 30-bit width is to support decode of traces that are captured by the on-chip buffer and subsequently unloaded by a JTAG tool.)

Target System Requirements

The decoder has been designed to work with target systems meeting the following requirements:

Supported processor

- StarCore140 "Platform 2002"

Object files

- You must have access to the object files for the code which is executing on your target system.

Supported compilers

- Metrowerks CodeWarrior IDE version 5.5.xxxx, or a compiler which generates object files with an equivalent ELF object file format.

Headers

- You must provide MICTOR headers, as described in this guide, to connect the logic analyzer probes to the signals on your target system.

Equipment Required

Logic analysis system

You need an Agilent 16900-series or 1680/90-series logic analyzer.

Logic analyzer cards

The logic analyzer card(s) you use must support the speed of the bus you are probing.

The logic analyzer card(s) must provide enough channels to probe the headers on your target system.

Table 1 Logic analyzer channels required

Probing scheme	Number of channels
2, 4 or 8 MDO signals 1 MICTOR connector	32
16 MDO signals 2 MICTOR connectors	64
30 or 32 MDO signals 3 MICTOR connectors	96

Probes

You need an appropriate number of logic analyzer probes (“adapter cables”) to connect the logic analyzer cables to the headers on your target system. The probe must match the type of connector you have placed on your board. Agilent recommends a MICTOR connector and an Agilent E5346A or E5380A probe.

1 Introduction

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Designing Your Board

This chapter describes the factors you need to consider when designing and preparing your target system for logic analysis.

Overview of the Connectors

You must provide one or two AMP MICTOR 38 connectors with the signal mappings shown in the following sections. Use connector J1 if you have 16 or fewer data lines. Use connectors J1 and J2 if you have more than 16 data lines.

You may also need to provide a 2x10 berg connector for JTAG-only signals. See “Sharing the Connector Between Multiple Tools" on page 14 for more information on this connector.

Designing the Headers

AMP MICTOR 38 connectors

The signal-to-connector mappings shown in this chapter assume you are using AMP MICTOR 38 connectors.

Each MICTOR 38 connector carries 32 signals plus two clocks (CLK1 for two logic analyzer pods). Probes (part number E5346A, sometimes called “high-density termination cables”) are required to connect the logic analyzer cables to the MICTOR connector. These probes contain the required termination. One probe is required for every two logic analyzer pods.

To increase the structural support for the probes, you should use support shrouds on each connector.

For more information, including mechanical dimensions, see the *Agilent Technologies E5346A 38-Pin Probe and E5351A 38-Pin Adapter Cable Installation Note*, available from www.agilent.com.

Design Considerations

The connector must be close enough to the signal source so that the stub length created is less than $^{1}/_{5}$ the t_r (bus risetime). For PC board material, (er = 4.9) and Z_o in the range of 50 - 80Ω, use a propagation delay of 160 ps/inch of stub.

Each probed signal line must be able to supply a minimum of 600 mV to the probe tip and handle a minimum of 90 kΩ shunted by 10 pF. The maximum input voltage to the logic analyzer is ±40V peak

Signal-To-Connector Mappings

J1: Nexus signals for Agilent logic analysis and ARM RealView Trace

J1 is designed to be used either with an Agilent logic analyzer *or* with ARM's RealView Trace. When J1 is used with the logic analyzer, the JTAG (run control) signals (shaded in blue) must be routed to a separate JTAG-only connector (page 14) so they are accessible to a JTAG controller such as ARM RealView ICE.

The signals shaded in blue are used by RealView Trace, but are not used by the logic analyzer.

Analyzer Pod	Nexus Signal	Mictor pin # (top view)		Nexus Signal	Analyzer Pod
5V	NC	1	2	NC	I2C
5V	NC	3	4	NC	I2C
CLK even	NC-pulldown	5	6	MCKO	CLK odd
D15 even	DBGRQ[1]	7	8	MRDY or DBACK	D15 odd
D14 even	nSRST[1]	9	10	EVTI	D14 odd
D13 even	TDO[1]	11	12	VTRef	D13 odd
D12 even	RTCLK[1]	13	14	VSupply	D12 odd
D11 even	TCK[1]	15	16	MDO7	D11 odd
D10 even	TMS[1]	17	18	MDO6	D10 odd
D9 even	TDI[1]	19	20	MDO5	D9 odd
D8 even	nTRST[1]	21	22	MDO4	D8 odd
D7 even	MDO15	23	24	MDO3	D7 odd
D6 even	MDO14	25	26	MDO2	D6 odd
D5 even	MDO13	27	28	MDO1	D5 odd
D4 even	MDO12	29	30	NC-pulldown	D4 odd
D3 even	MDO11	31	32	EVTO	D3 odd
D2 even	MDO10	33	34	MSEO 1	D2 odd
D1 even	MDO9	35	36	MSEO 0	D1 odd
D0 even	MDO8	37	38	MDO 0	D0 odd

J2: Upper Nexus signals for logic analysis

This header is required only if the Nexus core is set up to collect more than 16 bits of data.

Analyzer Pod	Nexus Signal	Mictor pin # (top view)		Nexus Signal	Analyzer Pod
5V	NC	1	2	NC	I2C
5V	NC	3	4	NC	I2C
CLK even	NC	5	6	NC	CLK odd
D15 even	MDO31	7	8	NC	D15 odd
D14 even	MDO30	9	10	NC	D14 odd
D13 even	MDO29	11	12	NC	D13 odd
D12 even	MDO28	13	14	NC	D12 odd
D11 even	MDO27	15	16	NC	D11 odd
D10 even	MDO26	17	18	NC	D10 odd
D9 even	MDO25	19	20	NC	D9 odd
D8 even	MDO24	21	22	NC	D8 odd
D7 even	MDO23	23	24	NC	D7 odd
D6 even	MDO22	25	26	NC	D6 odd
D5 even	MDO21	27	28	NC	D5 odd
D4 even	MDO20	29	30	NC	D4 odd
D3 even	MDO19	31	32	NC	D3 odd
D2 even	MDO18	33	34	NC	D2 odd
D1 even	MDO17	35	36	NC	D1 odd
D0 even	MDO16	37	38	NC	D0 odd

Bus and signal descriptions

MDO Required. Data lines. This bus may be 8, 16, 30, or 32 bits wide.

MSEO Required. Start or End of Message. This bus may be 1 or 2 bits wide.

EVTO Required. A value of 1 on this signal indicates that a trigger event has occurred. 1 bit wide.

NC Pins 1, 2, 3, and 4 must be true no-connects. Other NC signals can be left floating (no connects), or used to measure other signals of interest.

Other signals Optional. **The decoder ignores the signals shaded in blue.** These signals are routed to the connector to allow the connector to be used by RealView Trace. See the ARM *RealView ICE User's Guide* for detailed information on the requirements for these signals. If you plan to use this connector with another tool, you must follow the design requirements specified for that tool.

These signals must be routed to a second, JTAG-only header so that they are accessible to a JTAG controller such as ARM's RealView ICE. See "Sharing the Connector Between Multiple Tools" on page 14 for a description of the second connector.

In addition, special consideration must be given to these signals so that the logic analyzer does not load them, such that they cannot be controlled by the JTAG controller. Use a 10 kΩ pullup resistor to avoid such loading. See the *Agilent Technologies E5346A 38-Pin Probe and E5351A 38-Pin Adapter Cable Installation Note* for information on how the probe loads the signals.

Sharing the Connector Between Multiple Tools

The standard header defined in this document is designed to be used with RealView Trace (JTAG run-control and trace) or a logic analyzer (trace only).

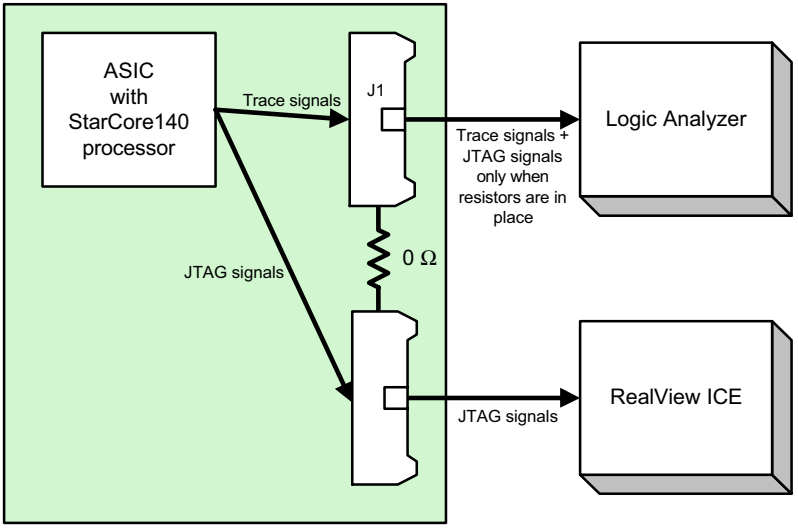
The logic analyzer ignores the JTAG signals. These signals must be routed to a second, JTAG-only header so that they are accessible to a JTAG controller such as ARM's RealView ICE. In addition, special consideration must be given to these signals so that the logic analyzer does not load them, such that they cannot be controlled by the JTAG controller.

See the ARM *RealView ICE User's Guide* for further information on the requirements for the JTAG signals. See the *Agilent Technologies E5346A 38-Pin Probe and E5351A 38-Pin Adapter Cable Installation Note* for information on how the probe loads the signals.

There are three possible ways to provide these signals to RealView ICE and at the same time, prevent the logic analyzer from interfering with their use.

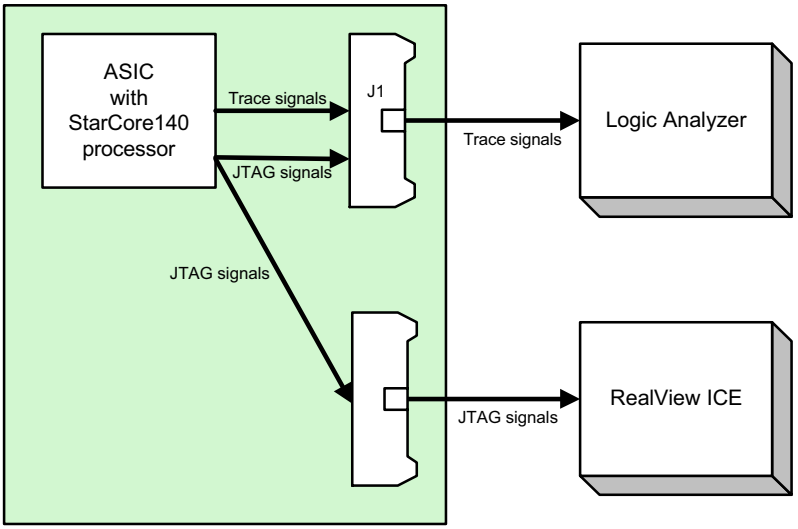
Option 1: Linked connectors

Route the JTAG signals to two connectors on the board: first to a JTAG-only 2X10 berg connector, then to J1. Place zero-Ohm resistors between the two connectors. Leave the zero-Ohm resistors in place when using J1 with RealView Trace. Remove the resistors when using J1 with the logic analyzer.



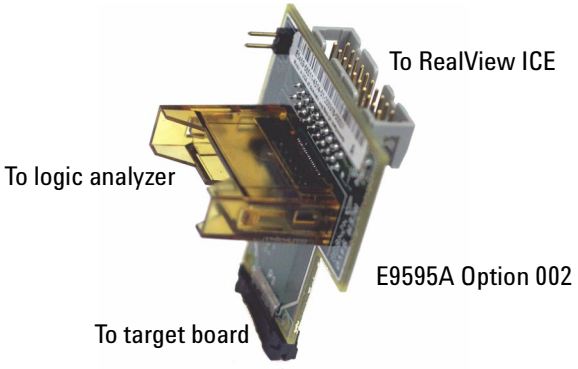
Option 2: Two separate connectors

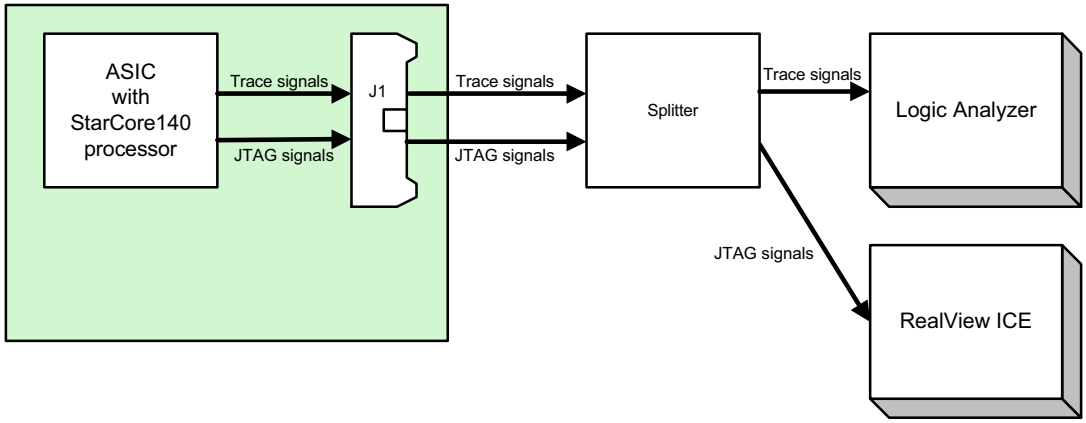
Route the JTAG signals to two connectors. Provide 10 kΩ pull-up resistors on the signals (particularly nSRST) so that the logic analyzer does not pull these signals to ground.



Option 3: Splitter board

Route the JTAG signals to one connector (J1) and use a splitter board such as Agilent product number E9595A Option 002 to provide the JTAG-only connector for RealView ICE.





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